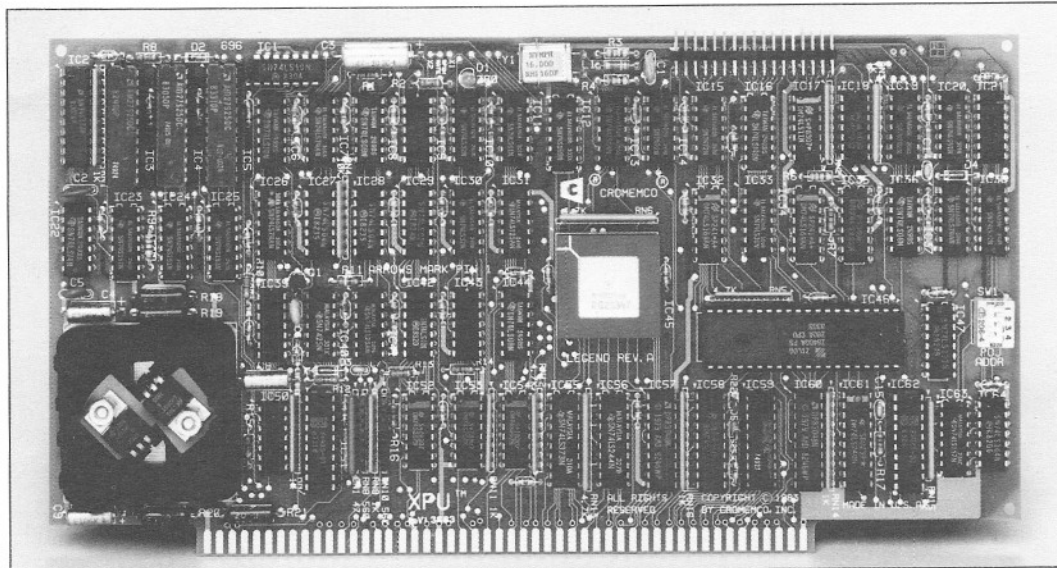


MODEL XPU Dual Processor Unit



FEATURES

- ☐ 68000 family processor with 32/16 bit operations
- ☐ Z-80A co-processor for software compatibility
- ☐ Supports full 16 megabytes of S-100 address space
- ☐ Separate 64K device address space for I/O
- ☐ Supports 128 interrupts on each processor
- ☐ Supports bus error and instruction resart
- ☐ Power-on jump to system bootstrap program
- ☐ Operates with XMM for memory-managed systems

The XPU is a twin-CPU board which offers the 68000 processor family and the Z-80A microprocessor for use in IEEE-696 (S-100) systems. The XPU offers full bus master capability, including such features as power-on jump to the bootstrap program, automatic generation of memory refresh signals, and hardware support of mixed 8-bit and 16-bit memory and I/O cards. The 68000 processor family includes seventeen 32-bit general purpose registers, a 32-bit program counter, a 16-bit status register, a 32-bit vec-

tor base register, and two 3-bit alternate function code registers. The processor can address 16 megabytes of memory using fourteen addressing modes, including direct, indirect, and auto-incrementing modes. The XPU supports a separate I/O address space of up to 65,536 devices. The Z-80A processor may be selected for operation at any time via a software command. The 68000 family then suspends its operation and allows the Z-80A to control the bus. In this manner the XPU can emulate perfectly the operation of Cromemco's original processor board, and run the large base of user-written software which exists for the Z-80. Processor selection is handled for the user automatically by the operating system. The XPU may be combined with the XMM memory manager to form a demand-paged, virtual memory machine. The 16 megabyte address space of the processor is mapped into pages of physical memory by the XMM. The instruction restart capability of the XPU is used to handle "page faults" and thus support virtual memory/machine systems.

TECHNICAL SPECIFICATIONS

Processors: 32 bit 68000 family and Z-80A

Memory Address Span: 16,777,216 bytes (68000)
65,536 bytes (Z-80A)

I/O Address Span: 65,536 devices (68000)
256 devices (Z-80A)

Bus Fault Recovery: Cycle restart on bus fault (68000)
Page faults handled by XPU/XMM combination
Supports ECC memory

Processor Selection: Software controlled by port 0FFH

Bootstrap: Power-on jump to Cromemco boot ROM

Byte/Word transfer: Handled by high-speed state machine for 68010

Vectored Interrupts: Supports 128 user interrupts per processor

Bus Interface: IEEE-696 (S-100)

Power Requirements: +8 volts @ 2.0 amps

Operating Environment: 0 to 55°C

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